REMARKS

The Examiner objected to claim 30 because of an informality. Applicant acknowledges that a typographical error had been introduced into the communication dated 31 July 2007. The error has been corrected, restoring the claim to its original form, as shown above.

The Examiner objected to claim 22 stating that it contained two sentences, the second of which the Examiner believed to be intended to be claim 23. Applicant does not understand the Examiner's objection, as claims 22 and 23 were presented in their original form, as intended. Claims 22 and 23 have therefore not been amended.

The Examiner rejected claims 1, 3, 4, 9, 10 and 11 under 35 U.S.C. 102(b) as being anticipated by Muir, *et al* (hereafter "Muir")(3,374,463). Applicant traverses the rejection.

Claim 1 requires that data is shifted from one set of circuit elements to other non-adjacent circuit elements outside the set in an interleaving pattern, said set including row-adjacent and column-adjacent ones of said circuit elements. The Examiner identifies the nodes of the circuit shown in Figure 2 of Muir as the circuit elements. The Examiner interprets column 8, lines 1-4 regarding the shifting of data along "diagonal paths" through the array of nodes as teaching the requirement concerning non-adjacent elements outside the set. The Examiner points to Figure 2 and the passage from column 7 line 8 to column 8 line 32 as teaching the requirement that the data shifting occurs in an interleaving pattern.

First, Applicant submits that the Examiner has not explained which nodes the Examiner is interpreting as the "set" of elements containing data to be shifted. Assuming that the Examiner interprets the nodes in row A as constituting the set, as this row contains the data that is subsequently shifted through the array, Applicant submits that a single row of nodes would not include row-adjacent and column-adjacent nodes, as required by the claim. However, if the Examiner interprets the nodes in multiple rows, say row A *and* row B, as the set of elements, Applicant submits that Muir does not teach the shifting of the data contained in rows A *and* B into other parts of the array, but merely the shifting of the data from row A

to row B, then row B to row C, and so on. Hence, Applicant submits that the claim limitation regarding the shifting of data from one set of row-adjacent and column-adjacent circuit elements to other elements outside the set is not taught by Muir.

Second, Applicant submits that the passage cited by the Examiner as teaching the interleaving of data, in fact, only teaches the shifting of data in intact form through the array of nodes. Muir teaches that data may be shifted by more than one node spacing as it passes from one row to the next; however, Muir does not teach any form of interleaving. Applicant draws the Examiner's attention to a standard definition of interleaving given in (www.dictionary.com) which is **to insert something alternately and regularly between the parts of** something else. Applicant submits that the term "interleaving pattern" in the general field of this invention means that some degree of layering, alternating, shuffling or interspersing of some portions of data in between other portions of data must exist. The shift and rotate circuitry taught by Muir does not involve any such layering, alternating, shuffling or interspersing of data.

Hence, Applicant submits that Muir does not anticipate claim 1 and the claims dependent therefrom.

Claim 3 depends from claim 1 and further requires that the circuit elements (to which the strobe line is coupled and to which it provides a strobe signal) are located in a first pair of adjacent rows of the array, and that an additional strobe line is coupled, and provides strobe signals, to circuit elements located in a second pair of adjacent rows of the array. The Examiner identifies "control leads" HR, HL, QR, and QL discussed in column 24, lines 5-57 as the first strobe line, and identifies group A, B, and C of Figure 11 as the circuit elements located in the first pair of adjacent rows . The Examiner points to Figure 11, identifying X1A and X1B, and X2A and X2B as the additional strobe line, and A18V, B19V etc. as the elements located in a second pair of adjacent rows. Applicant submits that the Examiner appears to be identifying the same rows of elements, row A and row B, as constituting both the first pair and the second pair of elements required by the claim.

Claim 4 depends from claim 1 and further requires that the first strobe signal is operable to shift data from one of said circuit elements in the first pair of adjacent rows to one of said circuit elements in the second pair of adjacent rows. The Examiner points to col. 24-25, lines 45-4 as providing this teaching, identifying X1A , X1B, X2A, X2B etc. as the first strobe signal. First, Applicant submits that the Examiner previously identified X1A , X1B, X2A, X2B as related to the additional strobe line, not the first strobe line, providing the first strobe signal. Second, Applicant submits that the cited passage does not teach the shifting of data from one **pair** of rows to another, but from one row at a time to an adjacent row. Hence, there are additional grounds for allowing claim 4.

Claim 10 depends from claim 1 through claim 9 and further requires that the buffer connected to at least one end of the array is configured to load the data into one of said circuit elements in at least a portion of at least two of the rows of the array. The Examiner points to Fig. 1 of Muir, identifying 101 as the buffer in question. The Examiner points to col. 6, lines 60-75 as providing the teaching. Applicant submits that the cited passage discusses the transfer of words from the memory 101 to one or more registers through the shift and rotate circuit that the Examiner identifies as the circuit elements required by the claim, but is silent as to which nodes in the array receive the data. Applicant submits that Muir teaches elsewhere (column 7, lines 41-44) that data are loaded into the top row of the array. Applicant submits that there is no teaching regarding any loading into **at least two of the rows** of the array as required by the claim. Hence, there are additional grounds for allowing claim 10.

The Examiner rejected claim 21 under 35 U.S.C. 103(a) as being unpatentable over Kanatake, *et al* (hereafter "Kanatake") (2002/009 2993) in view of Bartholomew. Applicant assumes the Examiner also intended to reject claims 22-32 under this heading. Applicant traverses the rejection of claims 21-32.

In regards to claim 21, the Examiner states that Kanatake discloses the limitations of the claim except for a system and method for shifting the data between non-adjacent ones of the light modulation elements in an interleaving pattern. The Examiner looks to Bartholomew for the missing teachings. The Examiner maintains that it would have been obvious "to include the use of non-adjacent elements and an interleaving pattern as taught by

Bartholomew in order to reduce the time necessary to shift through the SLM". Applicant disagrees with the Examiner's reading of Bartholomew as providing the missing teachings required to satisfy claim 21.

First, Applicant submits that the data shifting taught by Bartholomew does not occur between non-adjacent elements. The Examiner points to Figure 1 identifying transistors 45 and 51 as examples of the non-adjacent elements required by the claim. First, Applicant submits that the connection between the transistors 45 and 51 does not transmit the data with which Bartholomew is concerned. Input bit 1, for example, is connected directly to the same terminal of 51 that the connection from transistor 45 to which the Examiner points is connected, and this terminal does not provide either of the output bits. In fact, Bartholomew teaches (Abstract) that the elements containing the data being shifted are not the transistors but cells that contain two transistors each. Second, Applicant submits that not only the transistors to which the Examiner points (45 and 51), but the cells within which they exist (41 and 58) are adjacent as they are in adjacent rows and adjacent columns, and hence are diagonally adjacent.

Second, Applicant submits that the data shifting taught by Bartholomew does not occur in an interleaving pattern. As noted above with respect to claim 1, the term "interleaving pattern" in the general field of this invention means that some degree of layering, alternating, shuffling or interspersing of some portions of data in between other portions of data must exist. Bartholomew teaches a barrel shifter, which is understood (see, for example, http://en.wikipedia.org/wiki/Barrel_shifter) to be simply a digital circuit that can circularly shift a data word by a specified number of bits. The term does not imply any layering, alternating, shuffling or interspersing of some portions of the data in the word in between other portions of data in the word.

Hence, Applicant submits that the Examiner has failed to make a *prima facie* case for obviousness with respect to claim 21 and the claims dependent therefrom

Claim 23 depends from claim 21 and further requires that strobe signals are applied to strobe lines electrically coupled to respective ones of said light modulation elements to cause the data to be shifted between the non-adjacent ones of the light modulation elements. The

Examiner points to paragraph 41 of Kanatake as providing this additional teaching. Applicant submits that the lines cited by the Examiner concern the precise motion control of the pixel panel as a whole, and is irrelevant to the data that alters the light modulation elements in the pixel panel. Applicant submits that the Examiner has not pointed to any teaching concerning strobe lines or strobe signals in Kanatake, let alone signals that cause data shift between light modulation elements. The Examiner has not pointed to any teachings in the prior art regarding this additional limitation. Hence, there are additional grounds for allowing claim 23 and the claims dependent therefrom.

Claim 24 depends from claim 21 through claim 23 and further requires utilizing a ripple clock to control the timing of applying the strobe signals. The Examiner points to Figure 1 of Bartholomew as providing this teaching, stating that "the input bit 0 is carried to the next stage". Applicant submits that Bartholomew does not provide any teachings regarding a clock of any type, let alone a ripple clock. Applicant further submits that Bartholomew does not provide any teachings regarding timing control of any strobe signals. The Examiner has not pointed to any teachings in the prior art regarding this additional limitation. Hence, there are additional grounds for allowing claim 24.

Claim 26 depends from claim 21 through claim 25 and claim 23, and further requires that the strobe signals are applied to respective sets of the light modulation elements, at least one of the sets comprising one of the light modulation elements in at least a portion of at least two adjacent rows. The Examiner points to paragraph 0050 of Kanatake as providing this teaching. Applicant submits that the issue is not whether pixels exist " on adjacent consecutive rows" as taught in the cited passage, but whether these particular pixels as a set receive strobe signals that cause data to be shifted between them, as required by the claim. As noted above with respect to claim 21, the Examiner has not pointed to any such teaching. Claim 26 also requires that the data is shifted between the light modulation elements **in non-adjacent rows**. The Examiner looks to Bartholomew (Fig. 1; 45 to 51) for this additional teaching. Applicant submits that Figure 1 shows that transistors 45 and 51 are in adjacent rows. Hence, there are additional grounds for allowing claim 24.

Claim 28 depends from claim 21 through claim 25 and claim 23, and further requires that at least one of the sets of elements receiving a strobe signal comprises one of the light

modulation elements in at least two groups of orthogonally-adjacent ones of the light modulation elements, the at least two groups being positioned diagonally within the array with respect to one another. The Examiner points to element 40 of Kanatake, but Applicant assumes this was in error and that the Examiner intended to point to element 38, the pixel panel, as the set of light modulation elements. The Examiner points to figure 1 of Bartholomew, identifying cells 42 and 58 as two groups of orthogonally adjacent elements, and then points to figure 2 of Bartholomew, identifying contacts 24 and 31 as somehow indicating that the two groups are positioned diagonally in the array with respect to each other.

First, Applicant submits that while Figures 1 and 2 show that cells 42 and 58 contain orthogonally adjacent transistors, cells 42 and 58 are also shown as being orthogonally adjacent within the array. Applicant surmises that the Examiner may have intended to identify cells 41 and 58 as the groups in question, as these cells are positioned diagonally in the array, and include contacts 24 and 31 respectively. However, even in this case, The Examiner has not pointed to any teaching that cells 41 and 58 receive the same strobe signal, let alone one that causes data shifting as required by the claim. Hence, there are additional grounds for allowing claim 28.

Claim 29 depends from claim 21 and additionally requires that the data is loaded into the light modulation elements at one end of the array. The Examiner points to Figure 1 of Kanatake, identifying element 50 as providing the additional teaching. Applicant submits that element 50 is described by Kanatake (paragraph 0025) as simply a signal line carrying digital data to create a desired pixel pattern. Applicant further submits that the Figure merely indicates that there is a point of connection between element 50 and the pixel panel 38. Hence, Applicant submits that the Examiner has not pointed to any teaching that the data is loaded into the specific arrangement of elements at one end of the array. Accordingly, there are additional grounds for allowing claim 29 and the claims dependent therefrom.

Claim 32 depends on claim 21 through claim 29 and further requires that the loading comprises loading data into a first section of the array in response to a first strobe signal (input bit 1) derived from a second strobe signal (input bit 0) used to shift data in a second section of the array. The Examiner points to Bartholomew (col. 4, lines 5-67) as providing

this teaching, identifying input bit 1 as the first strobe signal and input bit 0 as the second strobe signal. Bartholomew teaches (column 2, lines 53-62) that input bits 1 and 0 are actually the data to be shifted. Applicant submits that these bits cannot also be strobe signals used to shift themselves. Hence, there are additional grounds for allowing claim 32.

The Examiner rejected claim 5 under 35 U.S.C. 103(a) as being unpatentable over Muir in view of Kanatake. Applicant traverses the rejection.

The Examiner states that Muir discloses the limitations of claim 1 but does not disclose the additional requirement of claim 5 that the strobe line is electrically coupled to one of said light modulation circuit elements located in at least a portion of at least two adjacent columns of the array. The Examiner looks to Kanatake (Fig. 1; 40, 32, 48, 38, 39, 54 and 55 and paragraphs 0043-0045) for the missing teachings. The Examiner maintains that it would have been obvious to modify Muir "to include the use of the light modulation circuit as taught by Kanatake in order to use light modulation" .

First, as noted above with respect to claim 1 from which claim 5 depends, Applicant submits that Muir does not teach that data is shifted from one set of circuit elements to other non-adjacent circuit elements outside the set in an interleaving pattern, said set including row-adjacent and column-adjacent ones of said circuit elements. Kanatake does not provide the missing teachings. At most, the cited passages and Figure 7 of Kanatake teach that data is shifted from one set of circuit elements to an adjacent set of circuit elements.

Second, Applicant does not understand the Examiner's suggestion that the system taught by Muir, a shift and rotate circuit for a data processor, would somehow be improved by using light modulation. Applicant submits that there is no suggestion of any need for light modulation in the circuit of Muir, and no obvious reason that light modulation would benefit such a circuit.

Hence, Applicant submits that the Examiner has failed to make a *prima facie* case for obviousness with respect to Claim 5.

The Examiner rejected claims 6, 7 and 8 under 35 U.S.C. 103(a) as being unpatentable over Muir, in view of Bartholomew. Applicant traverses the rejection.

The Examiner states that Muir discloses the limitations of claim 1 but does not disclose the additional requirement of claim 6 that the strobe line is electrically coupled to at least two groups of orthogonally-adjacent ones of said circuit elements, said at least two groups being positioned diagonally in the array with respect to one another. The Examiner looks to Bartholomew for the missing teachings. The Examiner maintains that it would have been obvious to modify Muir "to include the use of orthogonally-adjacent elements as taught by Bartholomew in order to reduce the time necessary to shift through the elements".

First, as noted above with respect to claim 1 from which claim 6 depends, Applicant submits that Muir does not teach that data is shifted from one set of circuit elements to other non-adjacent circuit elements outside the set in an interleaving pattern, said set including row-adjacent and column-adjacent ones of said circuit elements. Bartholomew does not provide the missing teachings.

Second, the Examiner points to Figures 1 and 2 of Bartholomew, identifying elements 42 and 58 as two orthogonally adjacent circuit elements, and identifying elements 24 and 31 as two groups of such circuit elements. The Examiner points to col. 1-2, lines 65-2 as providing the additional teachings required by claim 6. As noted above with respect to claim 28, Applicant submits that while Figures 1 and 2 of Bartholomew show that cells 42 and 58 contain orthogonally adjacent transistors, cells 42 and 58 are also shown as being orthogonally adjacent within the array. Applicant surmises that the Examiner may have intended to identify cells 41 and 58 as the groups in question, as these cells are positioned diagonally in the array, and include contacts 24 and 31 respectively. However, even in this case, The Examiner has not pointed to any teaching that cells 41 and 58 receive the same strobe signal, let alone one that causes data shifting as required by the claim.

Third, Applicant submits that the motivation suggested by the Examiner to modify the circuit taught by Muir to speed the processing time by dealing with sets of orthogonally-adjacent elements is flawed. The circuit taught by Muir already discloses (Figure 9) that the control lines identified by the Examiner as strobe lines are connected to orthogonally adjacent

elements in the array of nodes. Hence, there would be no need to apply Bartholomew to provide this feature.

Accordingly, Applicant submits that the Examiner has failed to make a *prima facie* case for obviousness with respect to claim 6 and the claims dependent therefrom.

The Examiner rejected claim 12 under 35 U.S.C. 103(a) as being unpatentable over Muir. Applicant traverses the rejection.

Claim 12 depends from claim 1 through claim 9 and further requires that the buffer comprises buffer elements, each of said buffer elements loading data into a respective portion of the array, said strobe line being within a second portion of the array and being connected to clock one of said buffer elements associated with a first portion of the array to load data into the first portion of the array. The Examiner states that Muir discloses all the limitations of claim 12 except for that regarding the clock. The Examiner maintains that it would have been obvious to modify Muir to include the use of a clock "as all circuitry needs some form of timing"

First, as noted above with respect to claim 1, Applicant submits that Muir does not teach that data is shifted from one set of circuit elements to other non-adjacent circuit elements outside the set in an interleaving pattern, said set including row-adjacent and column-adjacent ones of said circuit elements.

Second, the Examiner points to Figure 1 of Muir, identifying memory 101 first as the buffer, and then as the buffer elements. The Examiner points to column 6, lines 55-75 as teaching that each of the buffer elements loads data into a respective portion of the array 100. Applicant submits that the cited passage discusses the transfer of words from the memory 101 to one or more registers through the shift and rotate circuit that the Examiner identifies as the circuit elements required by the claim, but is silent as to any specific relationship between buffer elements in the memory 101 and particular portions of the array that receive the data. Applicant submits that while Muir teaches elsewhere (column 7, lines 41-44) that data are loaded into the top row of the array, Muir does not teach that this top row corresponds to one specific buffer element within the entire buffer 101.

Third, the Examiner points to figure 11, identifying lines X1A, X2A etc. connected to control lines X1, X2 etc. as the strobe line. The Examiner has not pointed to any teaching that these lines are within a "second portion of the array' distinct from the portion into which data is loaded from the buffer.

Fourth, the Examiner suggests that it is inherent in any electronic circuitry that some form of timing is required, and hence, one can assume that lines X1A, X2A etc. are connected to clock one buffer element to load data into a first portion of the array. Applicant submits that the issue is not whether any form of timing is required for circuitry to operate but whether the action of **clocking** is taught by Muir, let alone the specific clocking of one buffer element associated with a first portion of the array to load data into the first portion of the array. The Examiner has not pointed to any such teaching.

Hence, Applicant submits that the Examiner has failed to make a *prima facie* case for obviousness with respect to Claim 12.

The Examiner rejected claims 13, 14, 15, 16, 17, 18 under 35 U.S.C. 103(a) as being unpatentable over Muir in view of Kanatake. Applicant traverses the rejection.

The Examiner states that Muir teaches all the limitations of claim 13 except for requiring that the circuit elements are light modulation elements, said light modulation elements including memory elements configured to store the data and shift the data there between; and pixel controllers configured to alter the state of respective ones of said light modulation elements in response to the data stored in respective ones of the memory elements. The Examiner looks to Kanatake for the missing teachings. The Examiner maintains that it would have been obvious to "include the use of the light modulation circuit as taught by Kanatake in order to use light modulation".

First, as noted above with respect to claim 1, Applicant submits that Muir does not teach that data is shifted from one set of circuit elements to other non-adjacent circuit elements outside the set in an interleaving pattern, said set including row-adjacent and

column-adjacent ones of said circuit elements. Kanatake does not provide the missing teachings.

Second, as noted above with respect to claim 5, Applicant does not understand the Examiner's suggestion that the system taught by Muir, a shift and rotate circuit for a data processor, would somehow be improved by using light modulation. Applicant submits that there is no suggestion of any need for light modulation in the circuit of Muir, and no obvious reason that light modulation would benefit such a circuit.

Hence, Applicant submits that the Examiner has failed to make a *prima facie* case for obviousness with respect to Claim 13 and the claims dependent therefrom.

Claim 14 depends from claim 13 and further requires that the memory elements include two groups of the memory elements, the pixel controllers being controlled by the memory elements in an interleaving pattern. The Examiner points to Muir (Figure 2 and col. 7-8, lines 8-32) as teaching the interleaving pattern. The Examiner points to Figure 11 of Muir, identifying A and B as the two groups of memory elements. Applicant submits that A and B are simply two adjacent rows of elements; they do not in themselves form an interleaving pattern. Moreover, the Examiner has not pointed to any teaching that the control of the elements in these rows occurs in an interleaving pattern.

Hence, there are additional grounds for allowing claim 14.

The Examiner rejected claims 19 and 20 under 35 U.S.C. 103(a) as being unpatentable over Muir. Applicant traverses the rejection.

Claim 19 depends from claim 1 and further requires that the electronic circuit additionally comprises: additional strobe lines; and a shift register electrically connected to said strobe lines to apply the strobe signals sequentially thereto. The Examiner states that Muir teaches all the limitations of the claim except for the requirement that the strobe signals are applied sequentially. The Examiner maintains that it would have been obvious to modify Muir to "include the use of applying the strobe lines sequentially as demonstrated from Muir in order to shift the data through the nodes as stated (col. 4, lines 58-75 of Muir)".

First, as noted above with respect to claim 1, Applicant submits that Muir does not teach that data is shifted from one set of circuit elements to other non-adjacent circuit elements outside the set in an interleaving pattern, said set including row-adjacent and column-adjacent ones of said circuit elements.

Second, the Examiner points to Muir (col. 6, lines 5-25 and Figure 1), identifying shift/rotate control circuit 110, shift/rotate circuit 100 and registers 104-106 as the shift register required by the claim. Applicant submits that Figure 1 shows these elements as distinct elements, separated by other elements such as 102 and 103, and that they do not, separately or in combination, make up a shift register. The Examiner points to col. 4, lines 58-75 of Muir, noting that as "the bits are shifted out the right end to the next node and are not reinserted at the left end (beginning)" this is equivalent to a shift register. The issue here is whether the shift register applies the strobe signals to the strobe lines. The Examiner has not pointed to any such teaching.

Hence, Applicant submits that the Examiner has failed to make a *prima facie* case for obviousness with respect to claim 19 and the claims dependent therefrom.

Claim 20 depends from claim 19 and additionally requires that the shift register implements a ripple clock. The Examiner points to Figure 1 of Muir, identifying register selector 107 as the ripple clock. The Examiner points to Muir, col. 6; lines 17-25, as providing the relevant teaching. The cited passage teaches that the selector 107 can read data from one of the registers 104-105 and transmit it to an accumulator 108. According to the Examiner, as the accumulator can add two data words successively transmitted to it, it "thus functions as a ripple clock". While an accumulator can operate by a ripple carry mechanism, the Examiner has not pointed to any teachings of a ripple clock.

Respectfully Submitted,

Calvin B. Ward
Registration No. 30,896
Date: December 3, 2007

Agilent Technologies, Inc.
Legal Department, M/S DL429
Intellectual Property Administration
P.O. Box 7599
Loveland, CO 80537-0599
Telephone (925) 855-0413
Telefax (925) 855-9214